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EXAMINER	
IM, JUNGHWA M	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 07/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/972,855	SUGIZAKI, YOSHIAKI	
	Examiner	Art Unit	
	Junghwa M. Im	2811	

-- The MAILING DATE of this c mmunication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3,12,13 and 19-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3,12,13 and 19-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 3, 12, 19, 21, 22 and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Gurtler et al. (US 5424245), hereinafter Gurtler.

Regarding claim 3, Fig. 1 of Gurtler shows a semiconductor device comprising;

a first semiconductor chip (21) where a semiconductor element (24, 32; a multiple wiring layer) is formed;

a plurality of first connecting terminals (20) arranged on a semiconductor element formation surface side in the first semiconductor chip and connected electrically to the semiconductor element;

conductive members (28) buried in a plurality of through holes that go through the first semiconductor chip; and

a plurality of second connecting terminals (36) on the back of the first semiconductor chip, and connected electrically to the semiconductor element via the conductive member,

wherein at least one of the connecting terminals is coupled to the assembly board/module substrate (49), and

one of the connecting terminals is arranged be closer to the assembly board/module substrate and the average density of arrangement of the one of the first connecting terminals and

the second connecting terminals is lower than another of the first connecting terminals and the second connecting terminals.

In detail, Fig. 1 of Gurtler shows that the number of the second connecting terminals (six connecting bumps) is more than that of the first connecting terminals (three connecting bumps).

Note that the bottom the module substrate is mounted on an assembly board.

Regarding claim 12, Fig. 1 of Gurtler shows a semiconductor further comprising a second semiconductor chip (10) stacked on the first semiconductor chip (21), wherein at least portion of the connecting terminals (20) arranged on a stacked surface between the first semiconductor chip and the second semiconductor chip of the first connecting terminals (18) and the second connecting terminals in the first semiconductor chip is coupled to the second semiconductor chip.

Regarding claim 19, Fig. 1 of Gurtler shows the semiconductor wherein said at least portion of the plurality of connecting terminals comprising conductive bumps.

Regarding claim 21, Fig. 1 of Gurtler shows a semiconductor device comprising;

a first semiconductor chip (21) where a semiconductor element (24, 32) is formed;

a plurality of first connecting terminals (36) arranged on a semiconductor element formation surface side in the first semiconductor chip and connected electrically to the semiconductor element ;

conductive members (28) buried in a plurality of through holes that go through the first semiconductor chip; and

a plurality of second connecting terminals (20) on the back of the first semiconductor chip, and connected electrically to the semiconductor element via conductive members,

Fig.3; and connected electrically to the semiconductor element via the conductive members,

wherein at least one of the connecting terminals is coupled to an assembly board/ a module substrate (49)

some of the first connecting terminals of the second connecting terminals are distributed and arranged in the surface of the semiconductor chip, and power supply or a ground potential is to be applied to said some of the first and second connecting terminals (col. 3, lines 37-41).

Regarding claim 22, Fig. 1 of Gurtler shows a semiconductor further comprising a second semiconductor chip (10) stacked on the first semiconductor chip (21), wherein at least portion of the connecting terminals (20) arranged on a stacked surface between the first semiconductor chip and the second semiconductor chip of the first connecting terminals (18) and the second connecting terminals in the first semiconductor chip is coupled to the second semiconductor chip.

Regarding claim 24, Fig. 1 of Gurtler shows the semiconductor wherein said at least portion of the plurality of connecting terminals comprising conductive bumps.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 3 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Maley (US 5424245).

Regarding claims 3 and 13, Fig. 1 of Gurtler shows a semiconductor device comprising;

a first semiconductor chip (220a) where a semiconductor element (an integrated circuit) is formed;

a plurality of first connecting terminals (connecting bumps) arranged on a semiconductor element formation surface side in the first semiconductor chip and connected electrically to the semiconductor element and that go through the first semiconductor (1-2) coupled to the second through n-th semiconductor chips (220n),

conductive members (246) buried in a plurality of through holes that go through the first semiconductor chip; and

a plurality of second connecting terminals (connecting bumps) on the back of the first semiconductor chip (flip chip arrangement; col. 2, line 21), and connected electrically to the semiconductor element via the conductive member,

wherein at least one of the connecting terminals is coupled to the assembly board/base substrate (202 in Fig. 10; col. 9, lines 62-64), and

one of the connecting terminals is arranged be closer to the assembly board/ base substrate and the average density of arrangement of the one of the first connecting terminals and the second connecting terminals is lower than another of the first connecting terminals and the second connecting terminals.

In detail, Fig. 13 of Maley shows that the number of the second connecting terminals (four connecting bumps in the second row from the bottom) is more than that of the first connecting terminals (three connecting bump in the first row from the bottom).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 20 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gurtler in view of Wenzel et al. (US 6150724), hereinafter Wenzel.

Regarding claim 20, Fig. 1 of Gurtler shows a semiconductor device comprising;

a first semiconductor chip (21) where a semiconductor element (24, 32; a multiple wiring layer) is formed;

a plurality of first connecting terminals (20) arranged on a semiconductor element formation surface side in the first semiconductor chip and connected electrically to the semiconductor element;

conductive members (28) buried in a plurality of through holes that go through the first semiconductor chip;

a plurality of second connecting terminals (36) on the back of the first semiconductor chip, and connected electrically to the semiconductor element via the conductive member,

a second semiconductor chip (10) stacked on the first semiconductor chip (21), wherein at least portion of the connecting terminals (20) arranged on a stacked surface between the first semiconductor chip and the second semiconductor chip of the third connecting terminals (18) and the second connecting terminals in the first semiconductor chip is coupled to the second semiconductor chip;

wherein at least one of the connecting terminals is coupled to the assembly board/module substrate (49), and

one of the connecting terminals is arranged be closer to the assembly board/module substrate and the average density of arrangement of the one of the first connecting terminals and the second connecting terminals is lower than another of the first connecting terminals and the second connecting terminals.

In detail, Fig. 1 of Gurtler shows that the number of the second connecting terminals (six connecting bumps) is more than that of the first connecting terminals (three connecting bumps).

Note that the bottom the module substrate is mounted on an assembly board.

Gurtler shows the most aspect of the instant invention except the limitation over the size of the first and second semiconductor chips. However, Fig. 5 of Wenzel shows a multi-chip packaging device wherein the second semiconductor chip (102) is larger than the first semiconductor chip (104).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Wenzel to the device of Gurtler in order to have the second chip larger than the first chip for better performance of the device.

Regarding claim 25, Fig. 1 of Gurtler shows a semiconductor device comprising;

a first semiconductor chip (21) where a semiconductor element (24, 32) is formed;

a plurality of first connecting terminals (36) arranged on a semiconductor element formation surface side in the first semiconductor chip and connected electrically to the semiconductor element ;

conductive members (28) buried in a plurality of through holes that go through the first semiconductor chip; and

a plurality of second connecting terminals (20) on the back of the first semiconductor chip, and connected electrically to the semiconductor element via conductive members; and connected electrically to the semiconductor element via the conductive members,

a second semiconductor chip (10) stacked on the first semiconductor chip (21), wherein at least portion of the connecting terminals (20) arranged on a stacked surface between the first semiconductor chip and the second semiconductor chip of the third connecting terminals (18) and the second connecting terminals in the first semiconductor chip is coupled to the second semiconductor chip;

wherein at least one of the connecting terminals is coupled to an assembly board/ a module substrate (49)

some of the first connecting terminals of the second connecting terminals are distributed and arranged in the surface of the semiconductor chip, and power supply or a ground potential is to be applied to said some of the first and second connecting terminals (col. 3, lines 37-41).

Gurtler shows the most aspect of the instant invention except the limitation over the size of the first and second semiconductor chips. However, Fig. 5 of Wenzel shows a multi-chip

packaging device wherein the second semiconductor chip (102) is larger than the first semiconductor chip (104).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Wenzel to the device of Gurtler in order to have the second chip larger than the first chip for better performance of the device.

Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gurtler in view of Maley.

Regarding claim 23, Gurtler shows the most aspect of the instant invention except n-th stacked chips. Fig. 13 of Maley shows the n-th stacked (220n) multi-chip device.

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Maley to the device of Gurtler in order to have n-th chips stacked for a compact packaging of the device.

Response to Arguments

Applicant's arguments with respect to the pending claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (571) 272-1655. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jmi

ORI NADAV
Patent Examiner